



Goddard Space Flight Center

HST SM4 Payload Operations Working Group #2
March 9, 2007



Bit Sync Assembly (BSA)
Operations Concept

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Bit Sync Assembly (BSA)

- **Bit Sync Assembly (BSA)**

- Eliminates single point hardware availability concerns
- Maintains core bit sync functionality provided by heritage Aydin PC335 ISA cards
 - Heritage Aydin PC335 ISA cards are re-packaged in dedicated chassis
 - Hardware configuration capability is provided via ISA interface at power on and via external Astronaut requests via switches
- BSA design is compatible with existing shuttle harnesses and interfaces
- Minimized size/volume of bit sync hardware required to be carried to orbit
 - Eliminates overhead associated with IBM 755 general purpose computer
 - No longer require:
 - » IBM 755 ThinkPad
 - » OnSite Expansion Chassis
 - » Windows 3.1 Operating System and associated diskettes
 - » HPGSCA Aydin software



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Bit Sync Assembly (BSA)

- **Minimized Risk**

- Utilizes heritage Aydin PC335 ISA cards
 - HST has four flight worthy Aydin PC335 bit sync cards in stock which will be integrated into self contained BSA units

- **New Hardware**

- BSA Controller board is responsible for configuration of Aydin card following power on or Astronaut request via switch interface
 - Design uses SEU immune Actel SX72 FPGA
- BSA Power supply uses modern high reliability radiation hardened International Rectifier DC/DC Converter
 - Concern previously raised by Crew that old HPGSCA power supply design was deemed low reliability/high risk
- Smaller package, single all-in-one unit design



Bit Sync Assembly (BSA)

- **Design Improvements**

- Reduce ‘care and feeding’ required by crew
- SEU reset option when Watchdog is enabled (can be manually disabled via front panel)
 - Heritage Aydin bit sync card is susceptible to SEU hits
 - BSA Controller design is immune to SEU hit due to use of SEU immune FPGA controller and radiation hardened power supply
 - Eliminates need for daily routine of installing/removing turn around plugs and associated data cable connect/disconnect operations
- Auto rate mode selection capability when enabled
 - If enabled and following loss of Frame Sync, BSA controller card will evaluate incoming input data rate and configure Aydin card accordingly (Refer to Controller Card logic flow diagram for details)
- Heritage data Y cable will now be a 1 to 1 cable with easy to mate circular connectors on both ends (instead of two heritage D connectors)

- **Ease of Use**

- Minimal user interfaces switches
- Status provided to front panel via LEDs
- Does not require complicated time consuming re-boot procedure
 - Reset button or Power Cycle

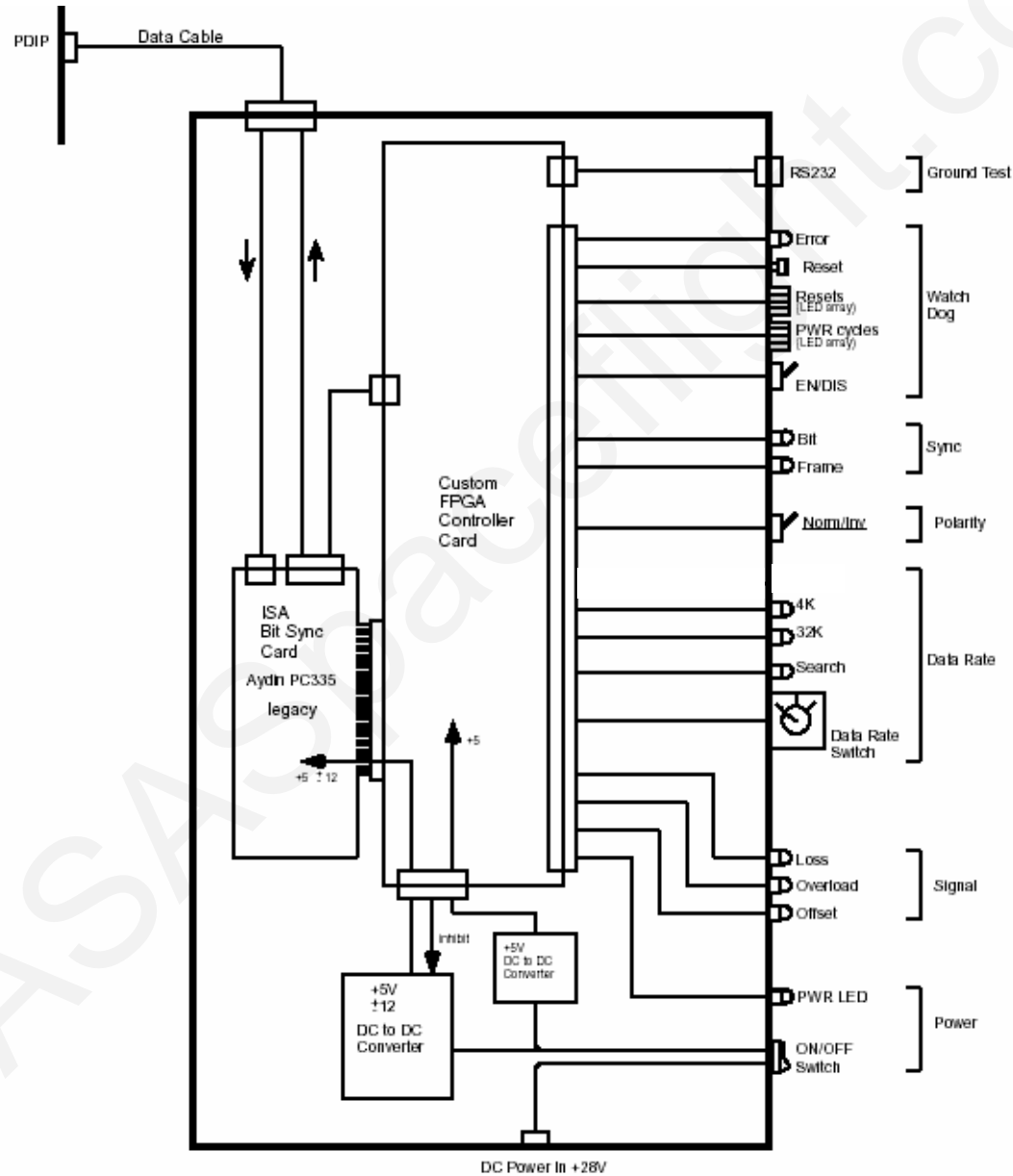


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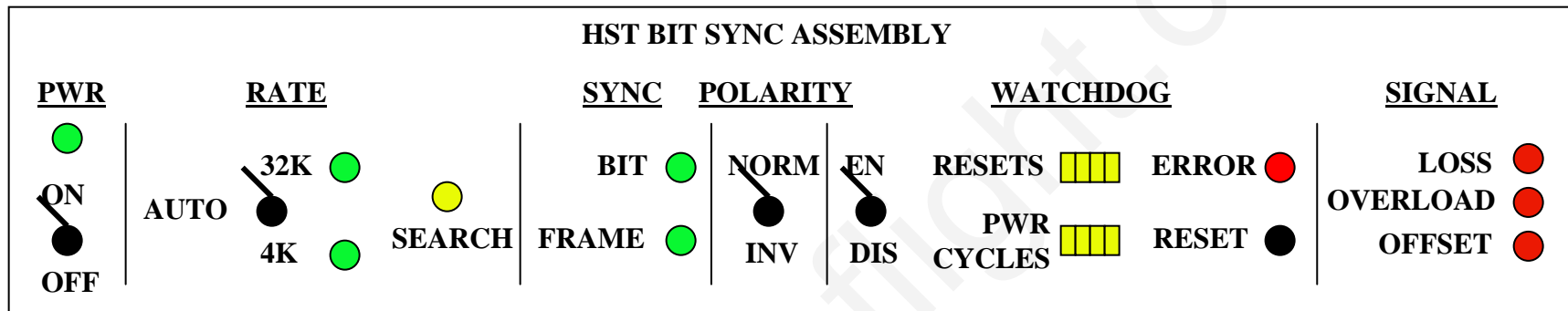


Bit Sync Assembly (BSA) Block Diagram





Bit Sync Assembly (BSA) Front Panel Diagram



RATE

32K: Aydin card configured for 32 kbps
Auto: Switch center position. Upon loss of Frame lock, BSA will select and configure Aydin bit rate based on sampled input data rate
4K: Aydin card configured for 4 kbps
Search: If yellow, indicates BSA sampled input data rate does not match present Aydin card configured rate

SYNC

Bit: If green, Aydin card has established a bit sync lock at selected rate
Frame: If green, BSA controller card has established an HST Telemetry Frame Header lock on the data provided by the Aydin card output

POLARITY

Norm: Aydin card configured to provide normal differential output data with respect to input data
Inv: Aydin card configured to provide inverted differential output data with respect to input data

WATCHDOG

En/Dis: Enable or Diable Watchdog feature
Resets: Binary counter of reset commands issued to Aydin card by watchdog since power up or reset
Pwr Cycles: Binary counter of power cycles executed by BSA controller since power up or reset
Error: If red, indicates BSA watchdog can not resolve out of lock condition and manual intervention is required
Reset: Momentary push button providing soft reset to BSA controller card

SIGNAL (Diagnostic)

Loss: If red, there may be no input signal or the input signal amplitude is smaller than the gain control circuit can accommodate
Overload: If red, the input signal amplitude is too great for the gain control circuit to accommodate and the bit sync is saturated
Offset: If red, the input signal has more offset than the correction circuit can accommodate

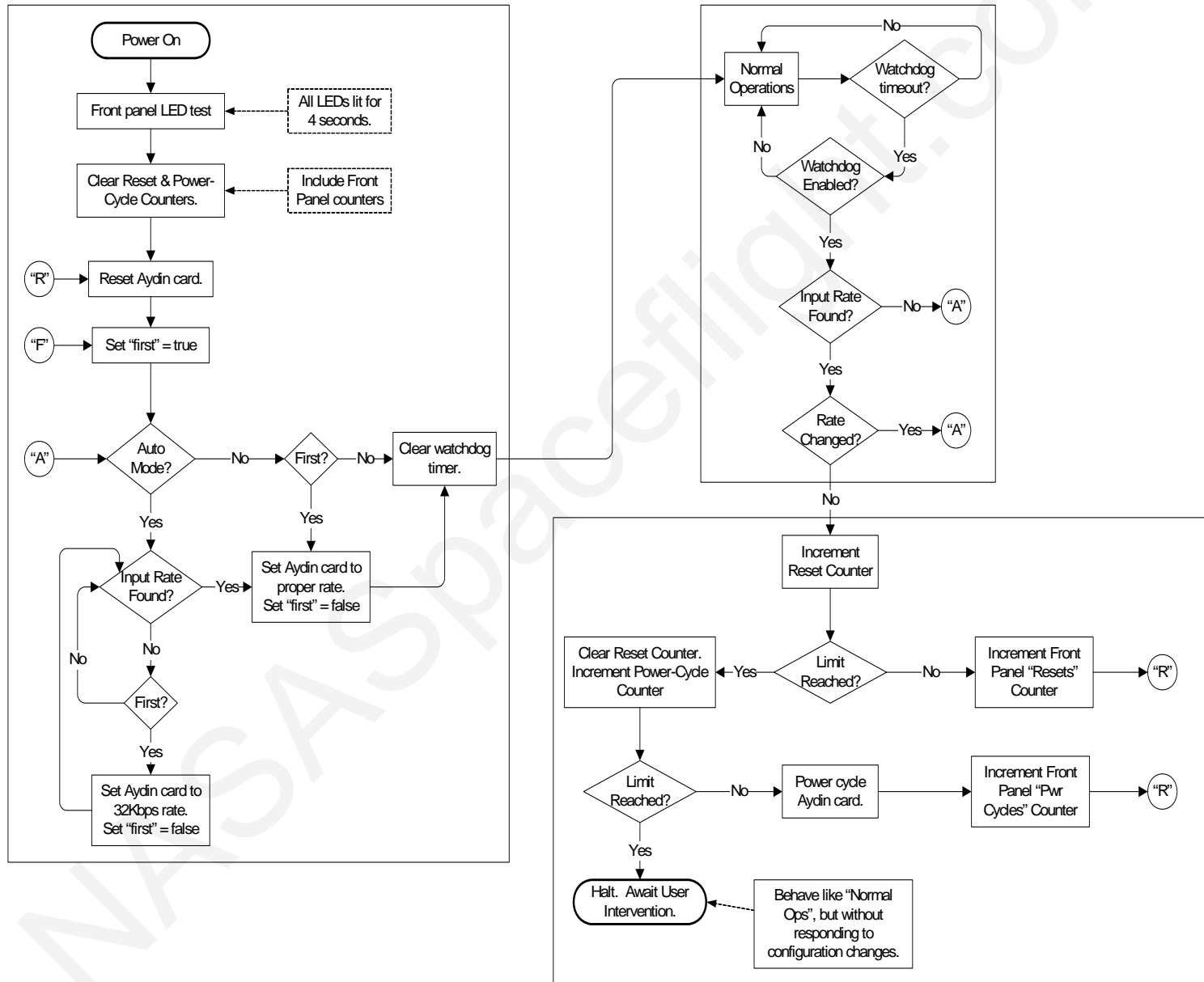


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Bit Sync Assembly (BSA) Logic Flow Chart



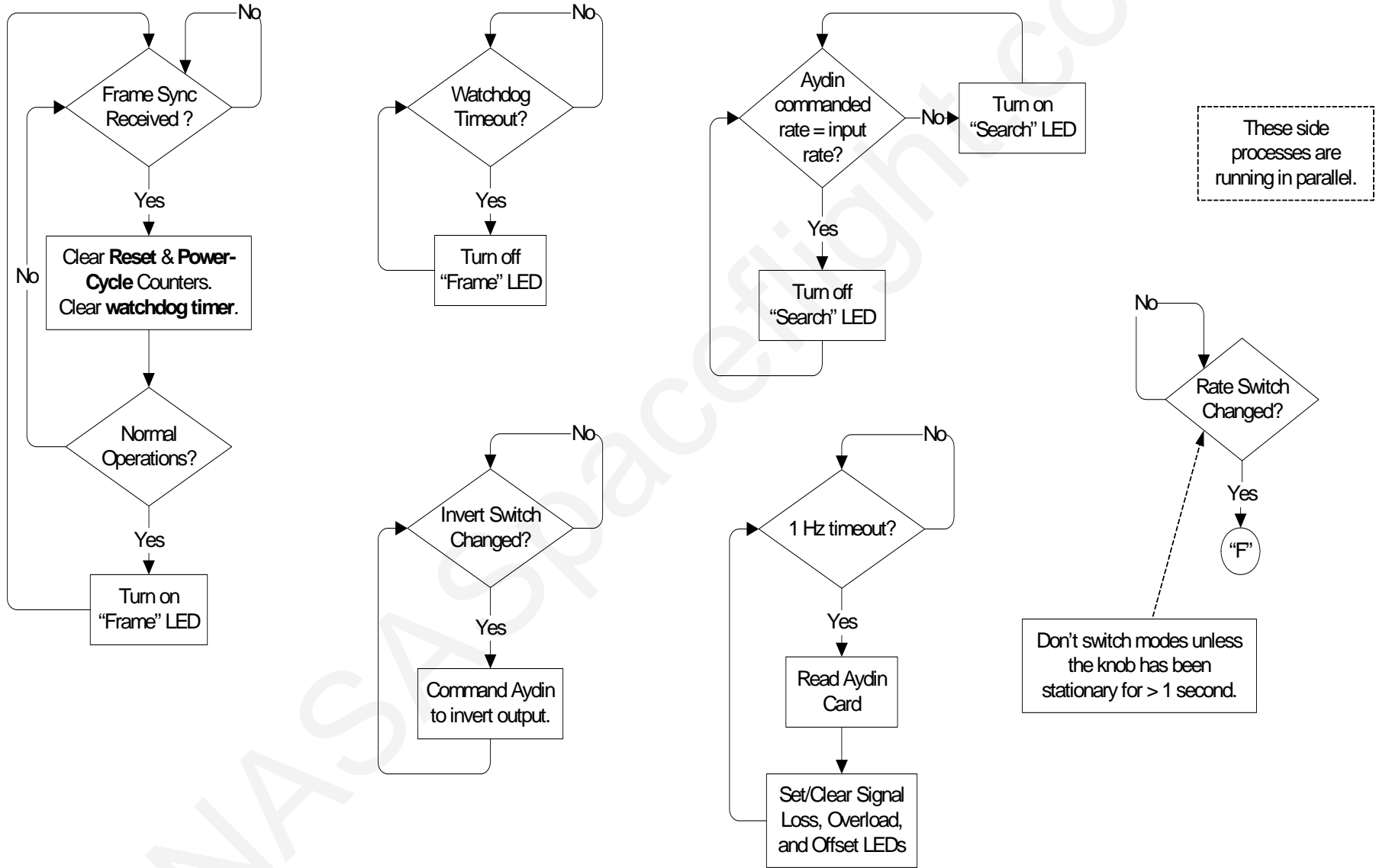


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Bit Sync Assembly (BSA) Logic Flow Chart





Pre-Rendezvous Operations

- **BSA Setup prior to HST Rendezvous (BSA Install & Config)**
 - Crew un-stows BSA Primary unit and associated data cable
 - BSA Redundant unit and redundant data cable remain stowed for contingency
 - Crew removes one PDIP turn around plug and mates data cable from BSA to PDIP panel
 - PDIP port #1 for PI #1 or PDIP port #2 for PI #2, depending on pre-selected primary PI from OPF testing
 - Crew mates +28V Power cable to BSA
 - Orbiter power source location pre-selected by Crew Compartment Stowage/Integration Team at JSC
 - Crew powers on BSA
 - Verify switches configured for 32K Rate, Normal, Watchdog Disabled
 - Switch on BSA Power
 - Perform visual LED verification (lamp test)
 - Verify Signal status LEDs are not red



Rendezvous, Docked, and Deploy Operations

- **BSA configured for manual-mode operations during rendezvous and berthing to facilitate troubleshooting (MAL 3.1a)**
 - RF link margin and multi-path effects due to PSP-bypass can drive undesired auto-operation
- **Auto-mode planned for use from first overnight through start of deploy operations**
 - INCO office approves in general
- **Manual-mode resumed for deploy through termination of PI comm operations (sep-2 burn)**
 - Same rationale as rendezvous
- **Breakdown and stowage per PL Ops (BSA Stow)**

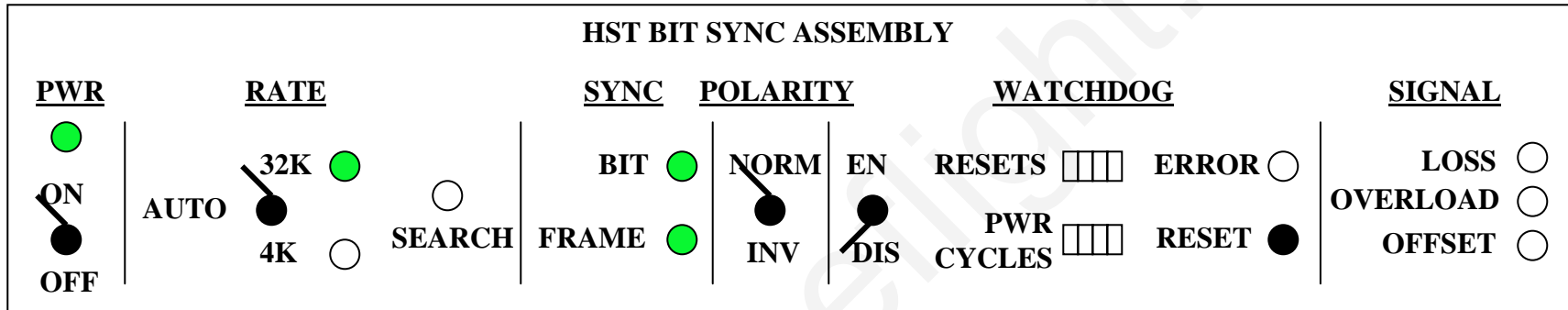


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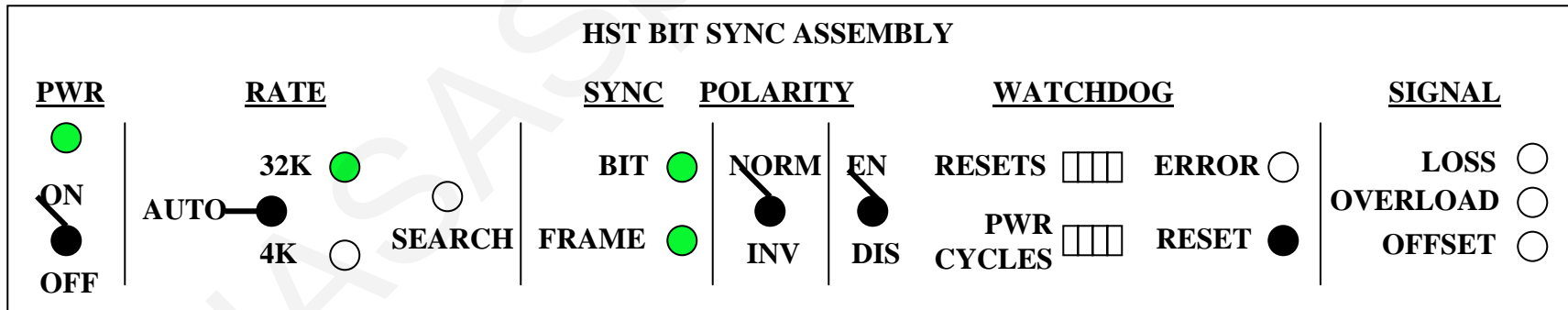


Bit Sync Assembly (BSA) Front Panel

HST Rendezvous and Deploy Ops



HST in Bay Ops





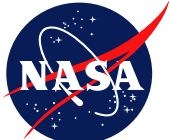
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BSA Schedule

- **BSA Schedule presently being re-baselined for 11 September 2008 launch date**
 - Delivery of four flight units, through environmental testing, by 12/7/07
 - Environmental testing will include EMI, 10.2 PSI Test, and Vib
 - Only two of the four BSA units will fly on SM4; one prime BSA and one contingency BSA
 - Flight Prime Bit Sync Cards:
 - » P/N PC335, S/N 6750-0101-2
 - » P/N PC335, S/N 6750-0101-4
 - Flight Spare Bit Sync Cards:
 - » P/N PC335, S/N 6750-0101-1
 - » P/N PC335, S/N 6750-0101-3
 - ESTL testing assumed to be L-6 months, followed by OPF testing at L-2 Months and PAD testing at L-4 to L-2 weeks
 - Engineering Model (EM) BSA unit:
 - Completion scheduled for August 2007
 - EM BSA will contain bit sync card P/N PC335, S/N 6750-0102-6



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